



Layout : Q87/B85H3-AM co-lay  
Schematic: Q87 only  
Rev:1.0

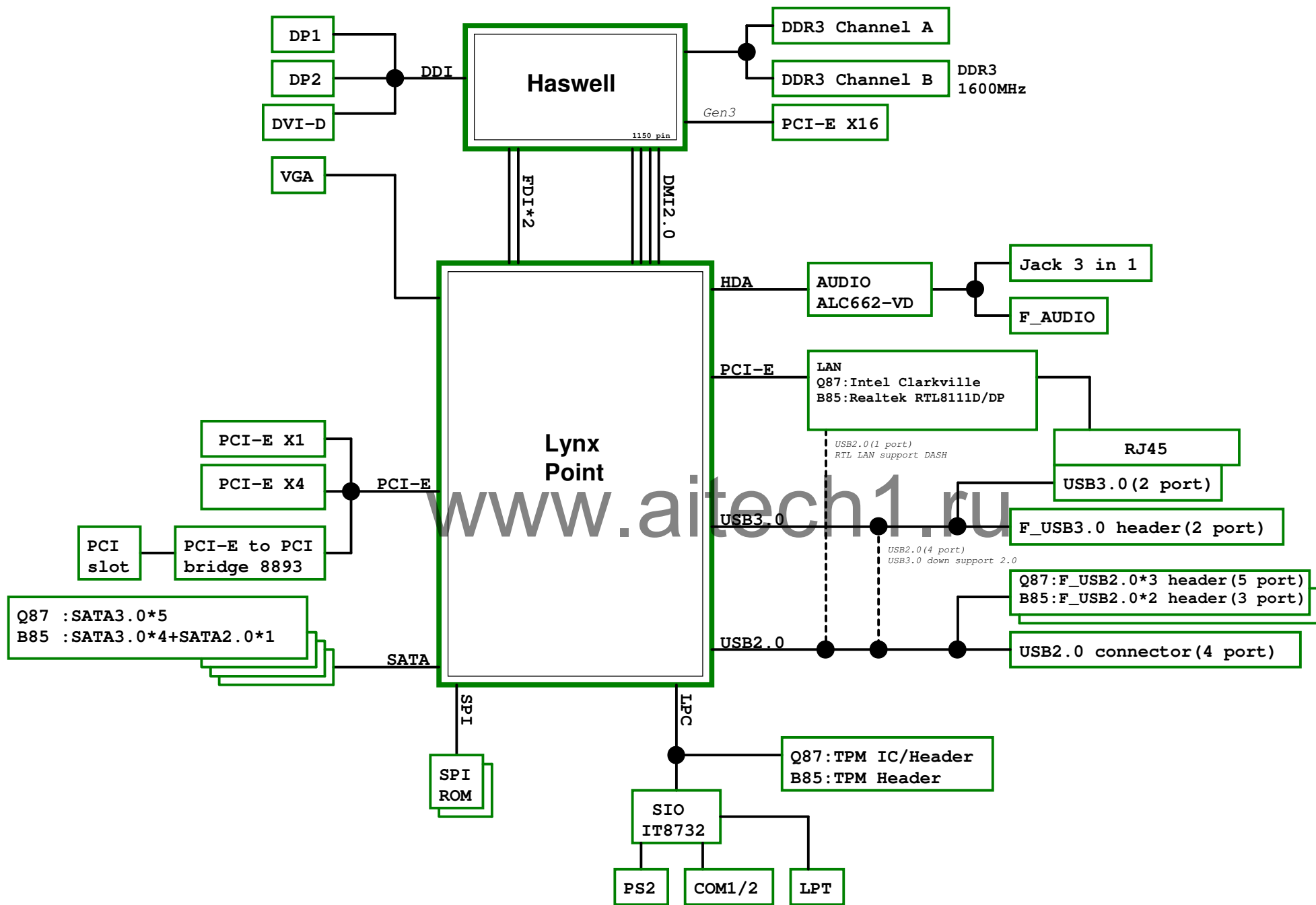
ECS  
CONFIDENTIAL

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REVISION HISTORY:

Rev	Date	Notes
27		ECIO-IT8732
28		FAN/PS2/Buzzer/F_Panel
29		LPT/COM/TPM
30		LAN Intel & Realtek
31		LAN+USB3.0 Connector
32		AUDIO-ALC662_VD
33		AUDIO-CONN & Header
34		XDP-CPU/PCH
35		DC/DC VDIMM/DDR_VTT/5VDUAL
36		DC/DC PCH_1.5V/PCH,ME_1.05V
37		DC/DC ATX_3VSB/3VDUAL
38		DC/DC Vcore /Gate driver
39		DC/DC VCC3 & VCC & ATX12P
40		PWR Delivery
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42		CLK Distribution



## PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO13	3VSB	LPC_PME	GPI
GPIO24	3VSB	USB_5VDUAL control (reserve)	GPO
GPIO72	3VSB	USB_5VDUAL control	Native
GPIO45	3VSB	BIOS WP	Native
GPIO57	3VSB	BIOS WP	GPI
GPIO46	3VSB	WLAN_DIS_L	Native
GPIO61	3VSB	LPCPD_L	Native
GPIO27	ATX_3VSB	ILAN_WAKE_L	GPI
GPIO1	VCC3	OBR	GPI
GPIO6	VCC3	Thermal_SD	GPI
GPIO68	VCC3	TP_VGA	GPI
GPIO23	VCC3	HDPANEL_DETECT	Native
GPIO15	3VSB	PEX16_RST	GPO
DL, BIOS must be pro			
GPIO73	3VSB	case open(reserve)	PCIECLKRQ0#
GPIO14	3VSB	ME_Disable	Native
GPIO19	VCC3	BOOT device detect	GPI
GPIO51	VCC3	BOOT device detect	GPO

## Interrupt mapping

Function	INT# port	PCIe*1 port	Device
PCI Bridge	INTA#	port 1	IC IT8893
mini-PCIE	INTB#	port 2	LPT integrate
LAN	INTC#	port 3	Clarkville or RTL8111DP
PCIEX1	INTD#	port 4	LPT integrate
PCIEX4	INTA#/B#/C#/D#	port 5~8	LPT integrate
SATA	INTB#	NA	LPT integrate

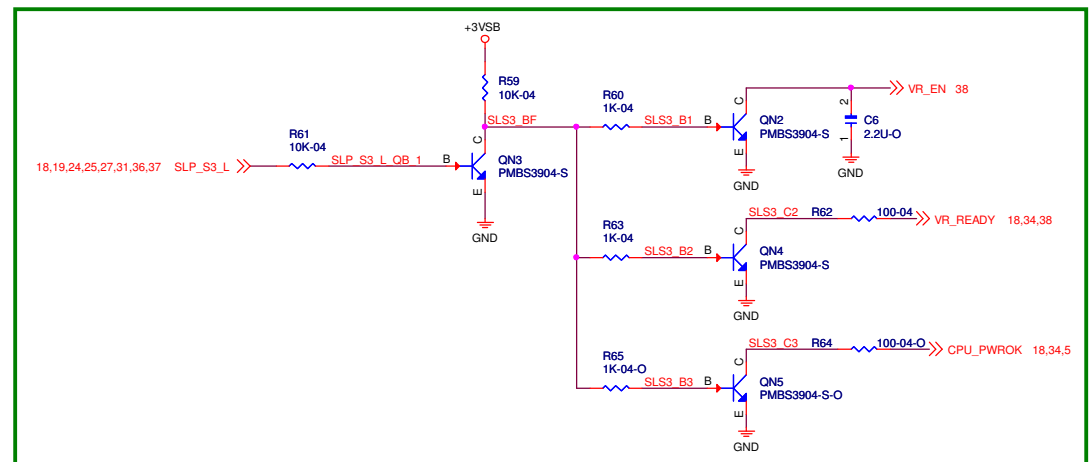
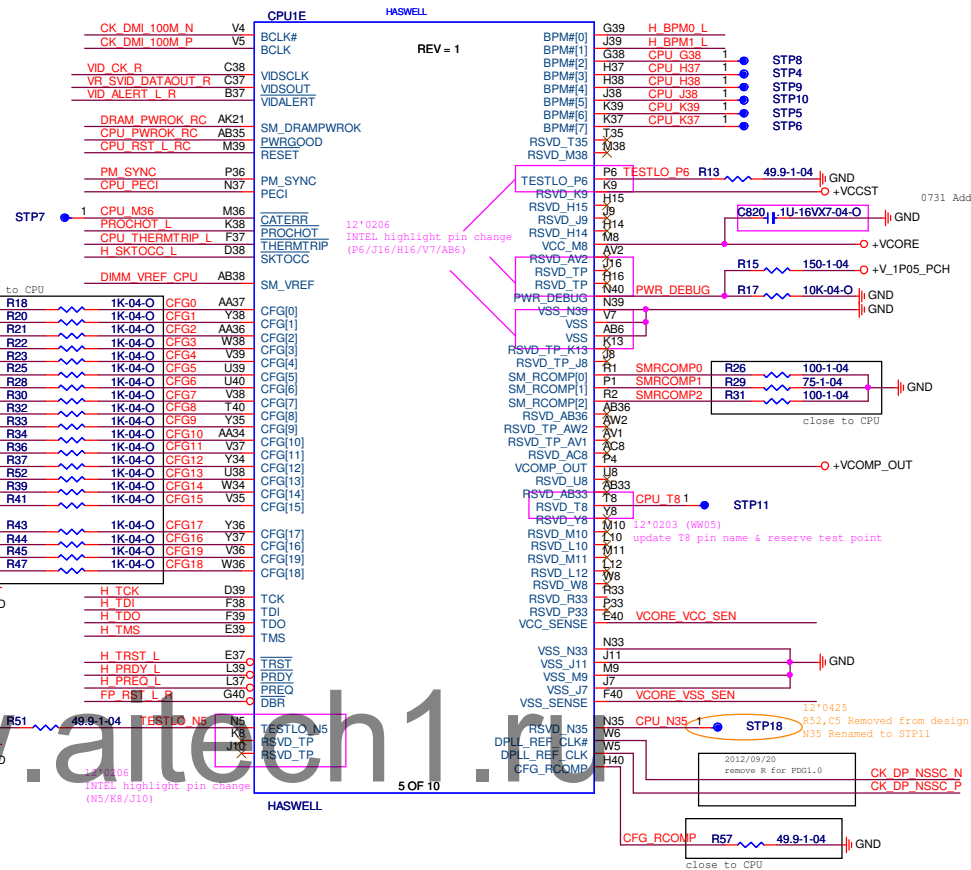
## SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP16	VCC3	Beep(reserve)	CIRR2
GP36	3VSB	Thermal_SD	FAN_CTL3
These GPIO pins are kept by VCC in default but can be changed to be kept by 3VSB if EC side writes 1 to 2012h[bit 5].			
GP35	3VSB	LED0	FAN_TAC4
GP37	3VSB	LED1	FAN_TAC3
GP70	VCC3	TPM Onboard detect	GPIO
GP71	VCC3	BOM detect	GPIO
GP73	VCC3	BOM detect	GPIO
GP74	VCC3	BOM detect	GPIO
GP76	VCC3	Thermal_HD_Auto_Switch	GPIO
GP46	3VSB	Acer Header	GPIO
GP47	3VSB	Acer Header	GPIO
GP40	3VSB	5VDUAL Switch	3VSBSW

BIOS must be pro to Native 3VSBSW

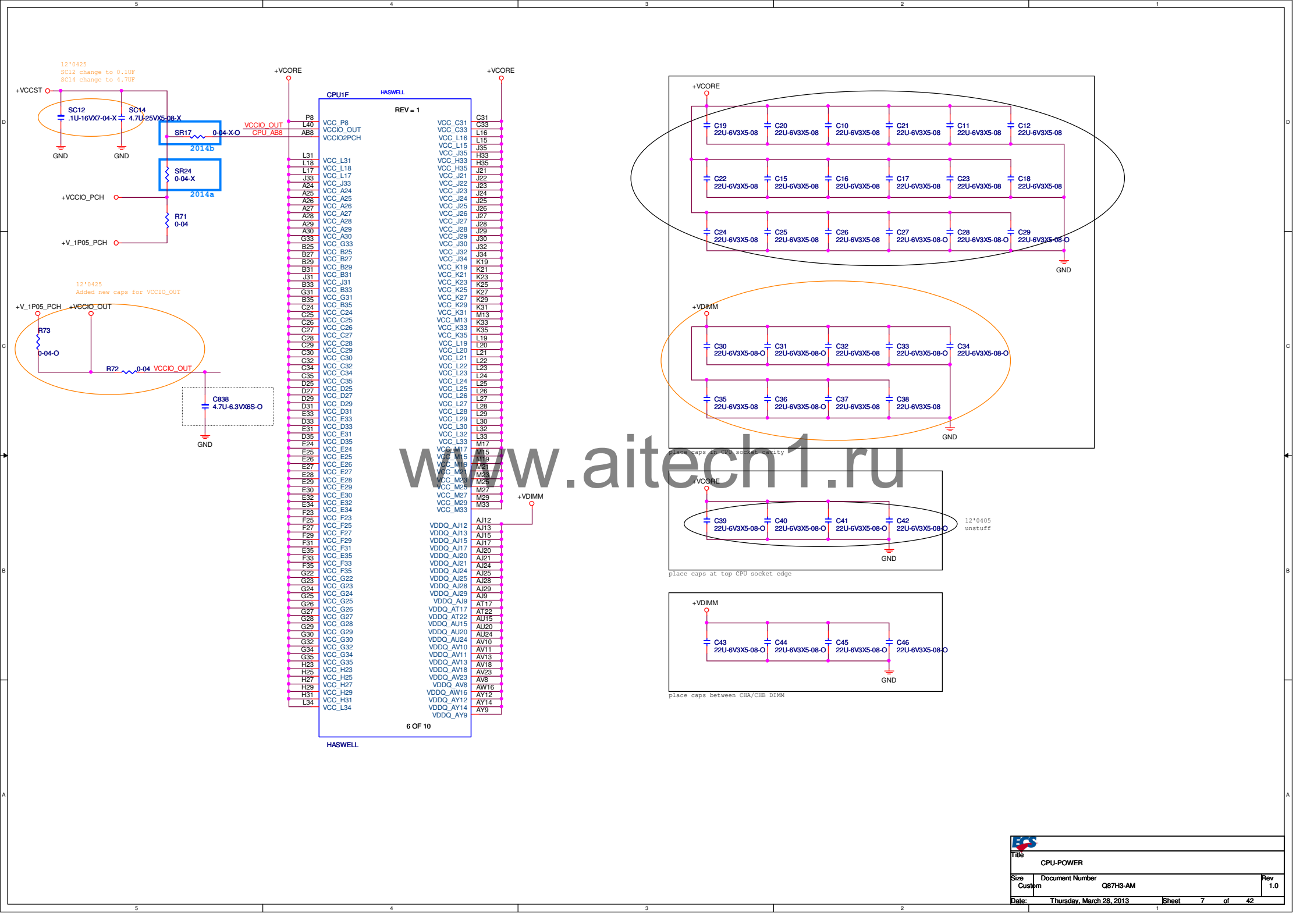




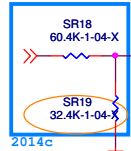


## Power Down Sequencing Circuit

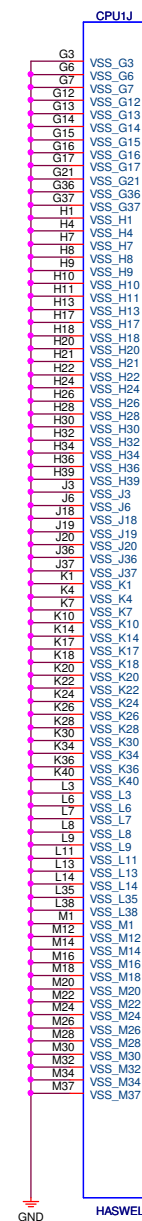
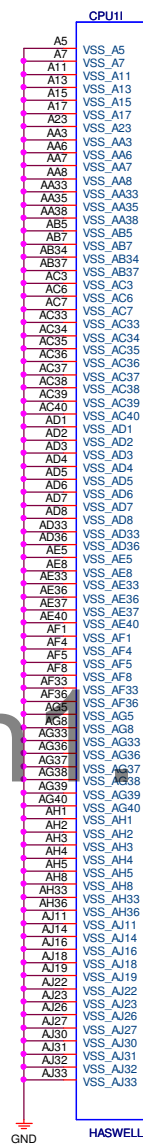
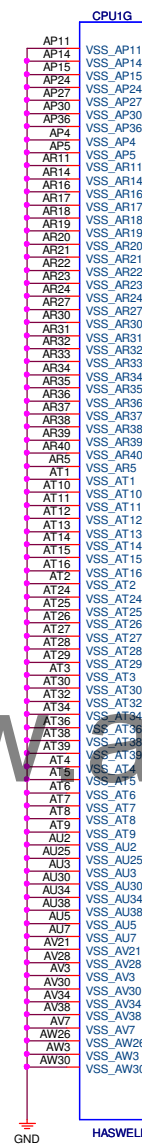
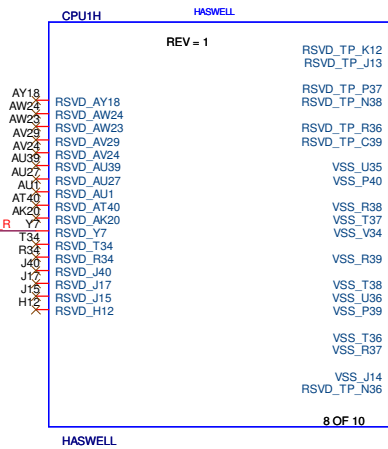




17,18,27,5 PCH\_PWROK

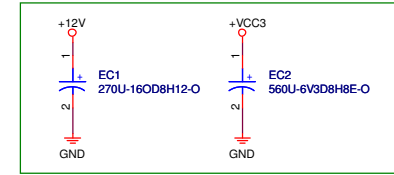
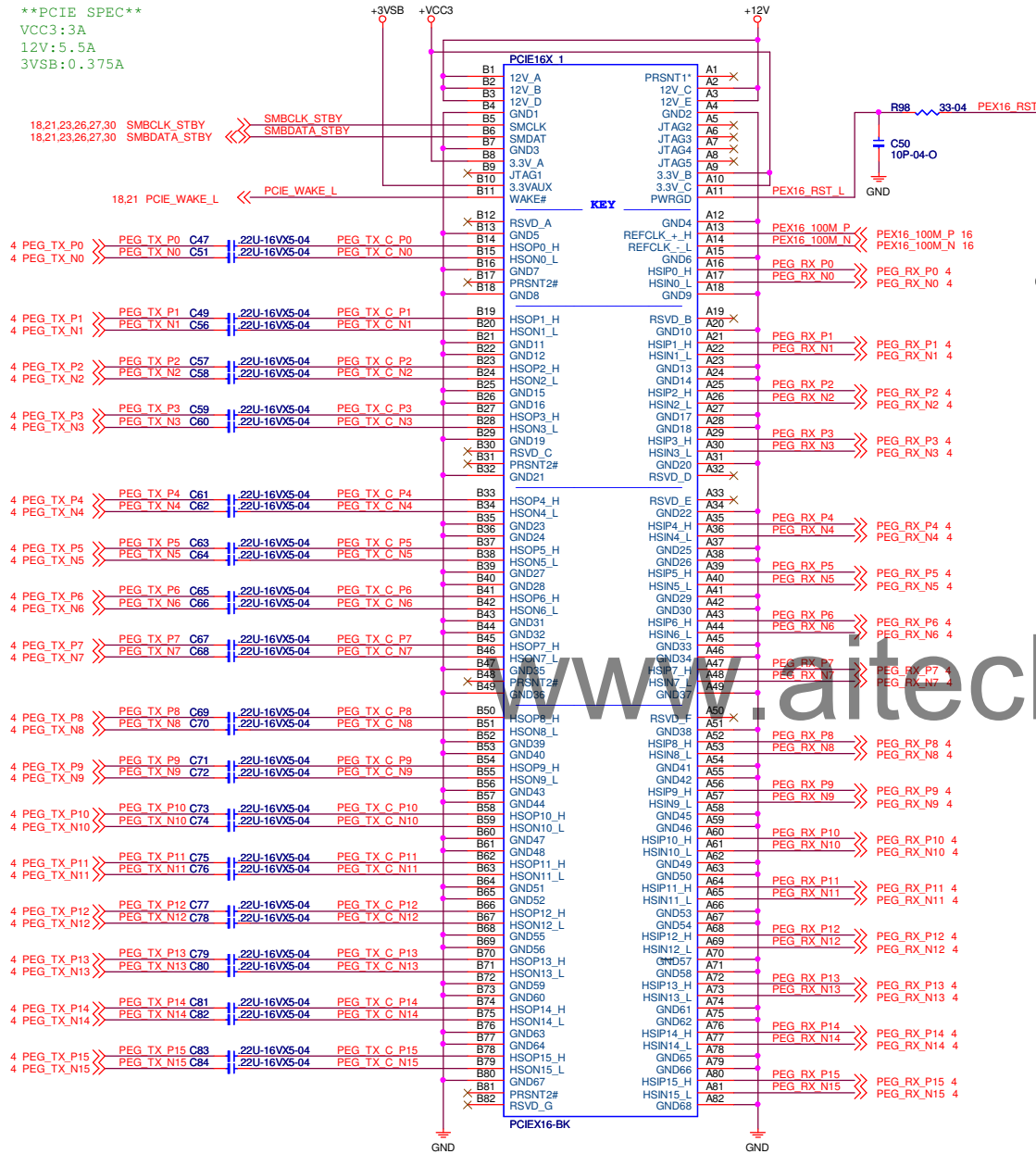


1210425  
SR19 change to 2.67K

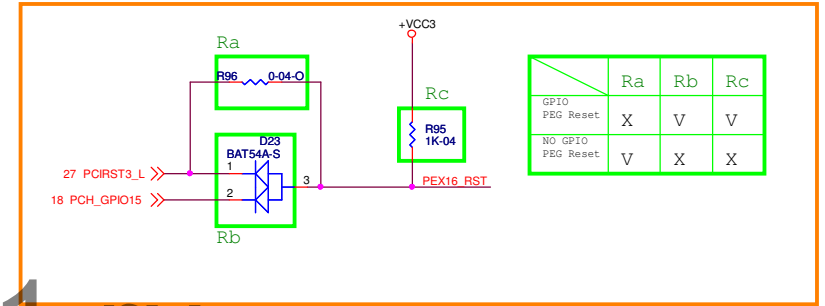
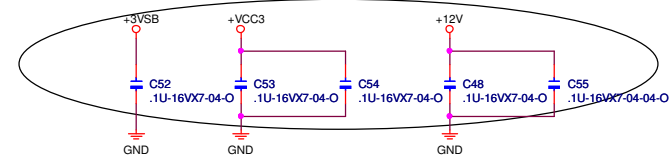


VSS\_NCTF\_AU40  
VSS\_NCTF\_AU39  
VSS\_NCTF\_AW38  
VSS\_NCTF\_AW37  
VSS\_NCTF\_AW36  
VSS\_NCTF\_AW35  
VSS\_NCTF\_AW34  
VSS\_NCTF\_AW33  
VSS\_NCTF\_AW32  
VSS\_NCTF\_AW31  
VSS\_NCTF\_AW30  
VSS\_NCTF\_AW29  
VSS\_NCTF\_AW28  
VSS\_NCTF\_AW27  
VSS\_NCTF\_AW26  
VSS\_NCTF\_AW25  
VSS\_NCTF\_AW24  
VSS\_NCTF\_AW23  
VSS\_NCTF\_AW22  
VSS\_NCTF\_AW21  
VSS\_NCTF\_AW20  
VSS\_NCTF\_AW19  
VSS\_NCTF\_AW18  
VSS\_NCTF\_AW17  
VSS\_NCTF\_AW16  
VSS\_NCTF\_AW15  
VSS\_NCTF\_AW14  
VSS\_NCTF\_AW13  
VSS\_NCTF\_AW12  
VSS\_NCTF\_AW11  
VSS\_NCTF\_AW10  
VSS\_NCTF\_AW09  
VSS\_NCTF\_AW08  
VSS\_NCTF\_AW07  
VSS\_NCTF\_AW06  
VSS\_NCTF\_AW05  
VSS\_NCTF\_AW04  
VSS\_NCTF\_AW03  
VSS\_NCTF\_AW02  
VSS\_NCTF\_AW01

\*\*PCIE SPEC\*\*  
VCC3: 3A  
12V: 5.5A  
3VSB: 0.375A



Between PCIe16 & PCIe1

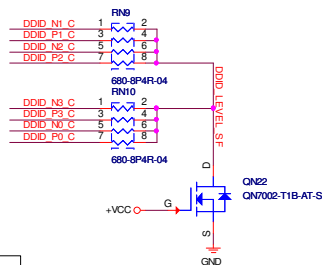
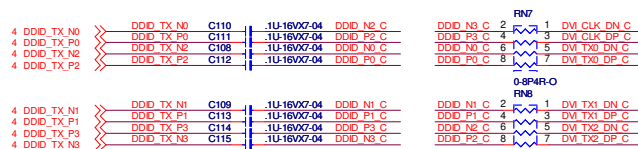


	Ra	Rb	Rc
GPIO PEG Reset	X	V	V
NO GPIO PEG Reset	V	X	X

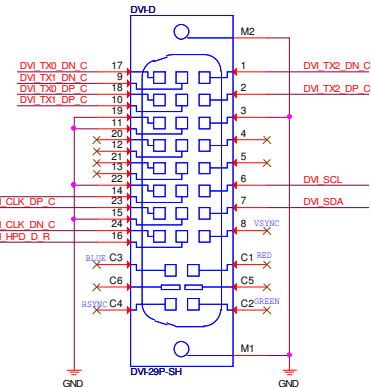
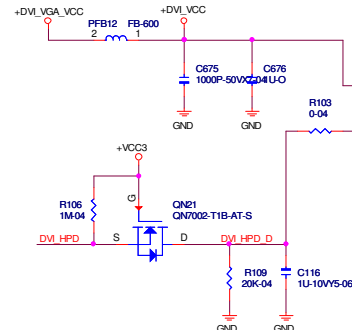
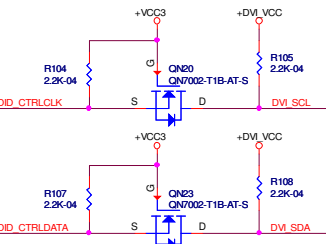
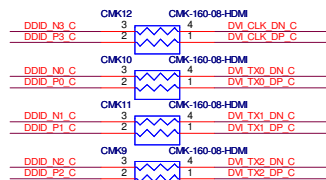
2012/7/05  
PCIe Gen3 slot reset circuit update .





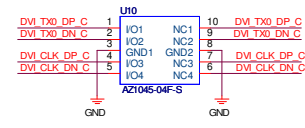
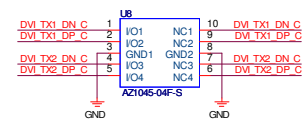


stitching caps for Bayenc/Vayenc



DVI-D conn  
 P/N: 10-025-024578 (KORTAK\_鍍殺+加高)  
 10-025-024694 (RI-TOP\_鍍殺+加高)

DVI-I conn  
 P/N: 10-025-029573 (KORTAK\_鍍殺)  
 10-025-029692 (RI-TOP\_鍍殺)  
 P/N: 10-025-029691 (KORTAK\_鍍殺+加高)  
 10-025-029691 (RI-TOP\_鍍殺+加高)

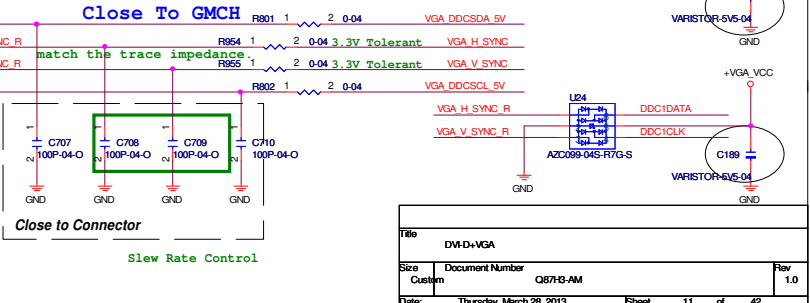
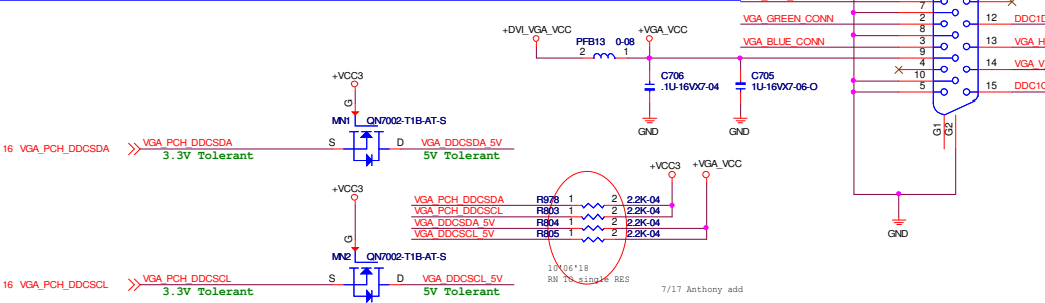
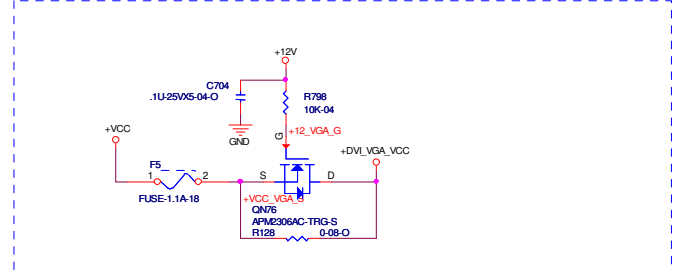
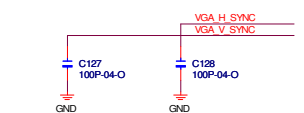
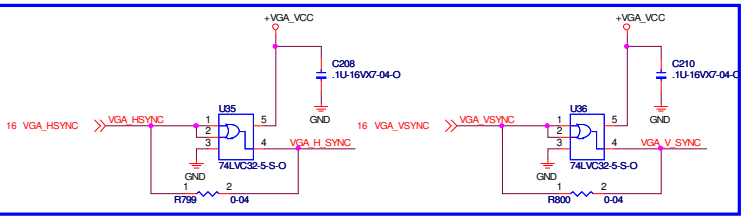
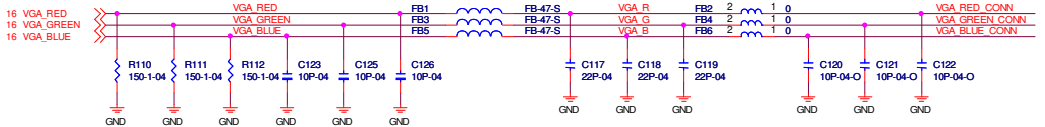


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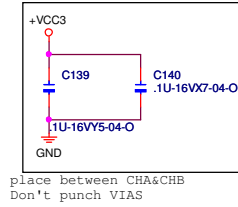
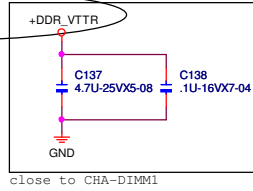
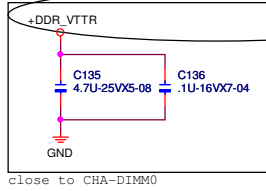
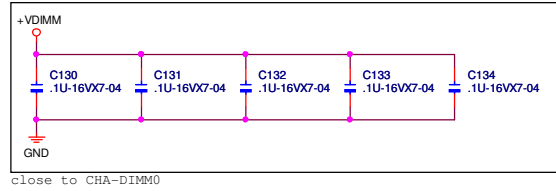
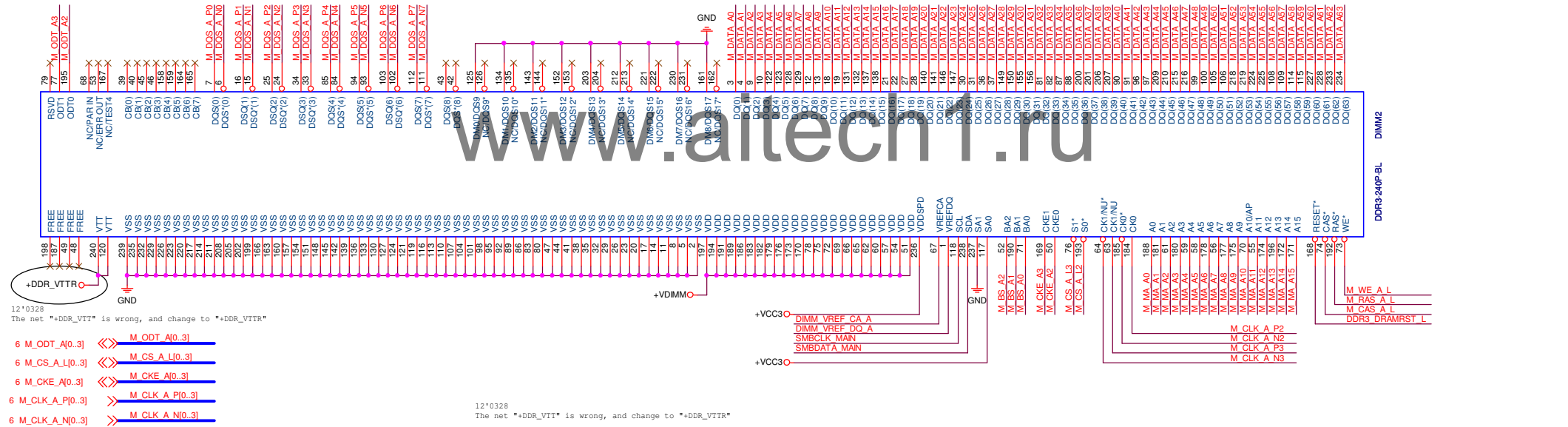
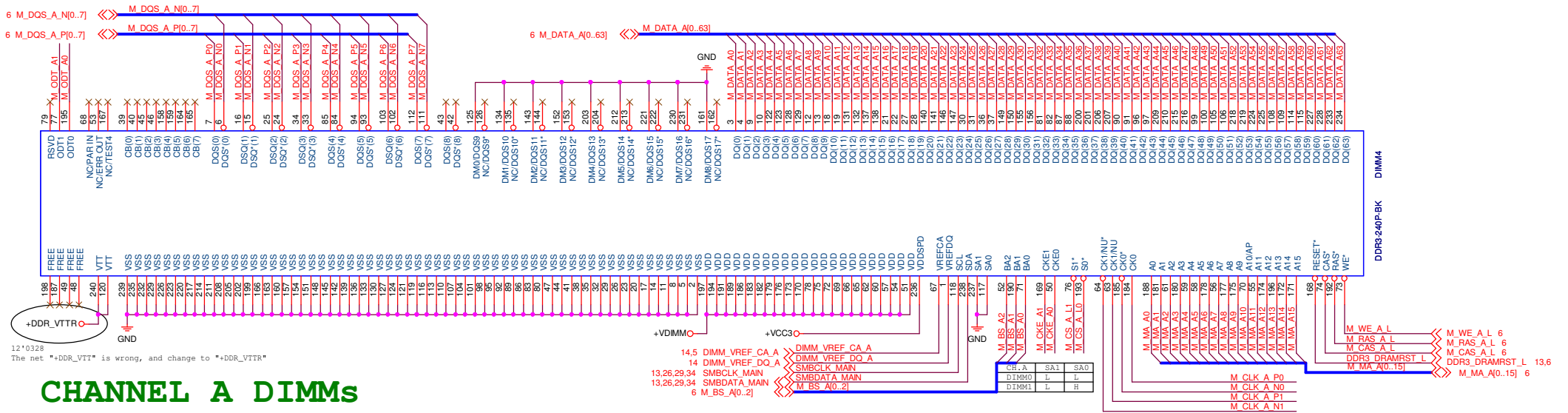
## DVI-D

## VGA

Board 47 01M  
 P/N: 16-101-470370

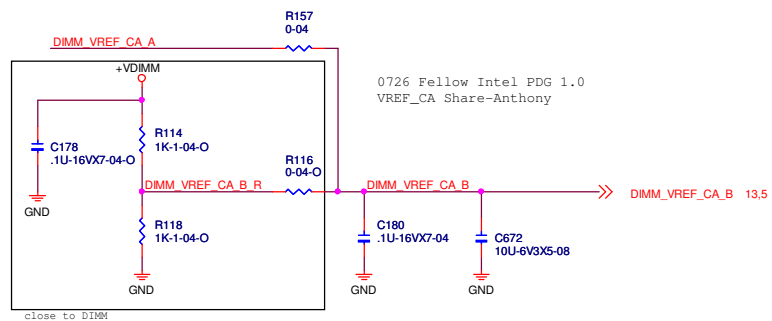
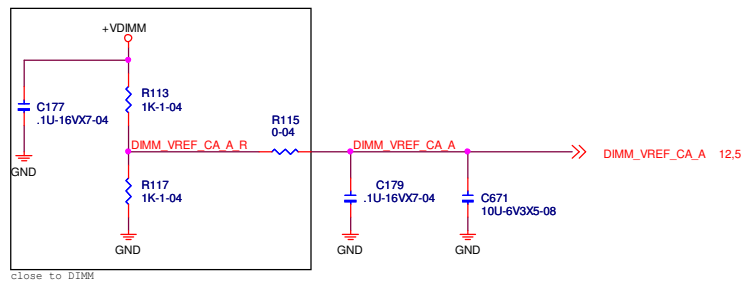


Title	DVI-D+VGA
Size	Document Number
Custom	Q8743-AM
Date:	Thursday, March 28, 2013
Sheet	11 of 42
Rev	1.0

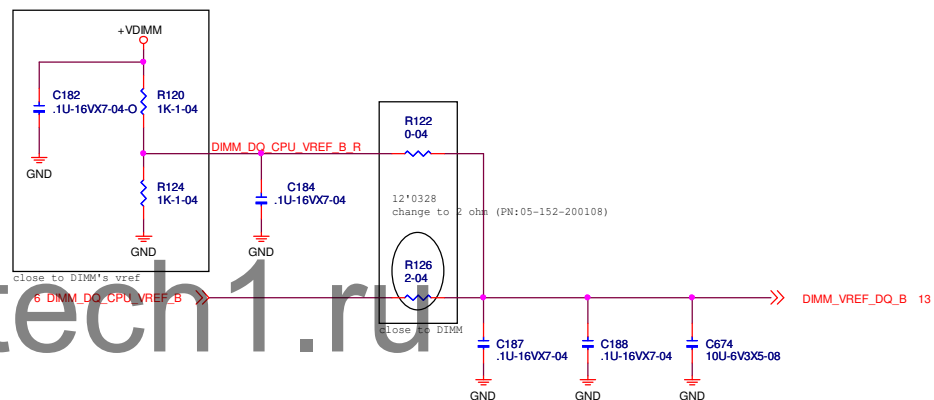
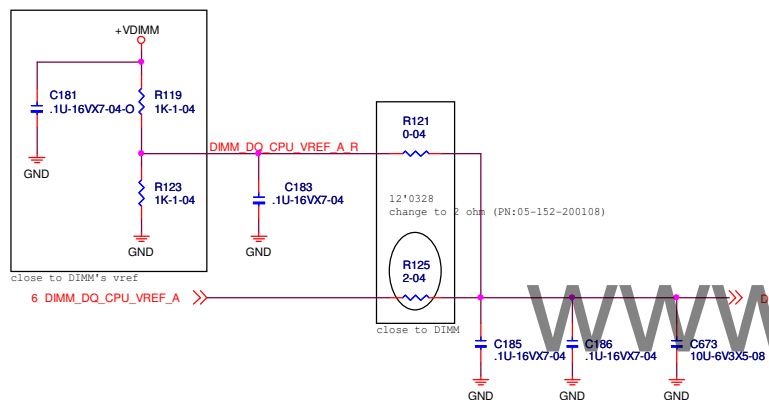






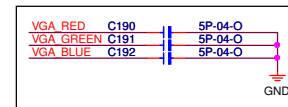
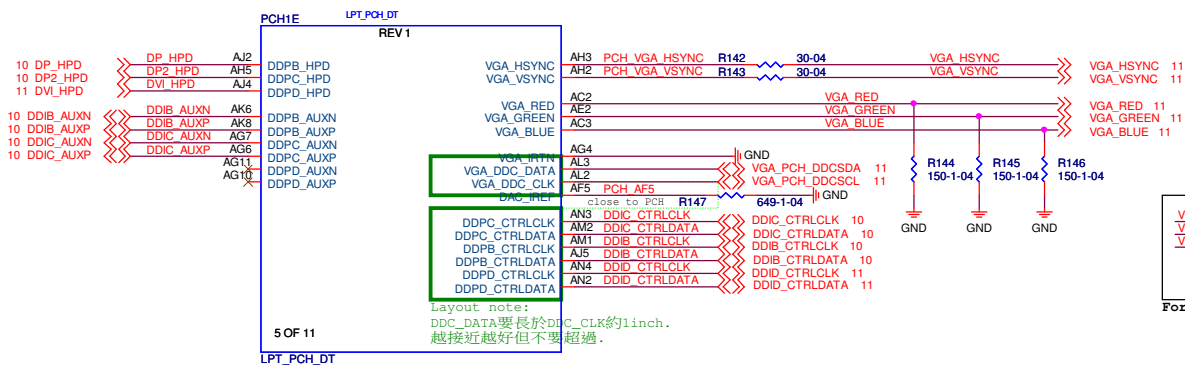


**DIMM\_VREF\_CA Circuit**

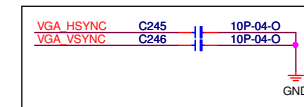


**DIMM\_VREF\_DQ Circuit**





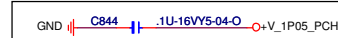
For EMI, close to chipset.



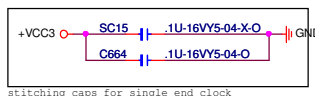
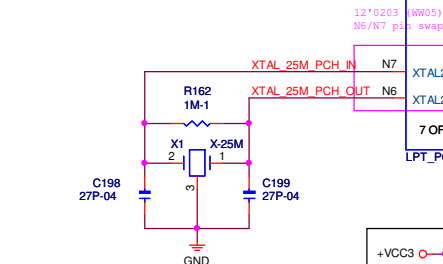
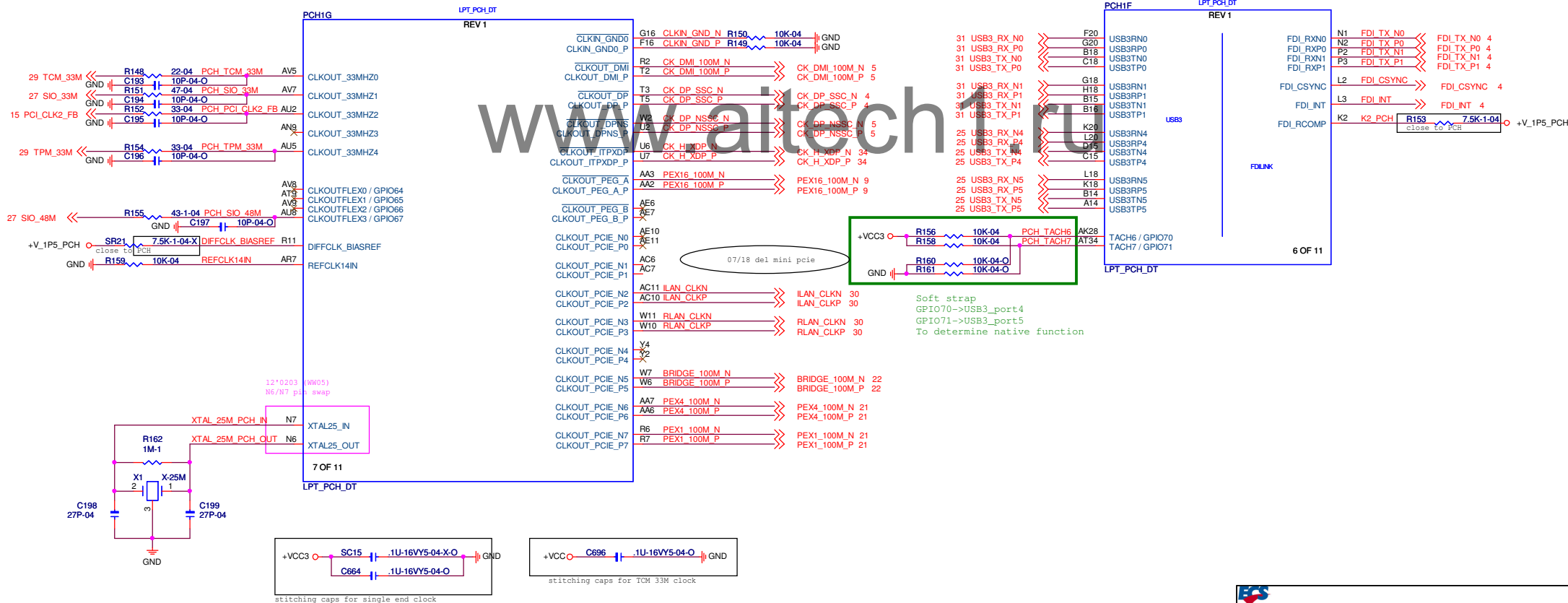
2012/07/09  
 Reserved Cap for Slew rate control



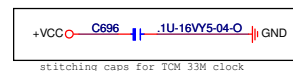
stitching caps for PCI\_CLK2\_FB



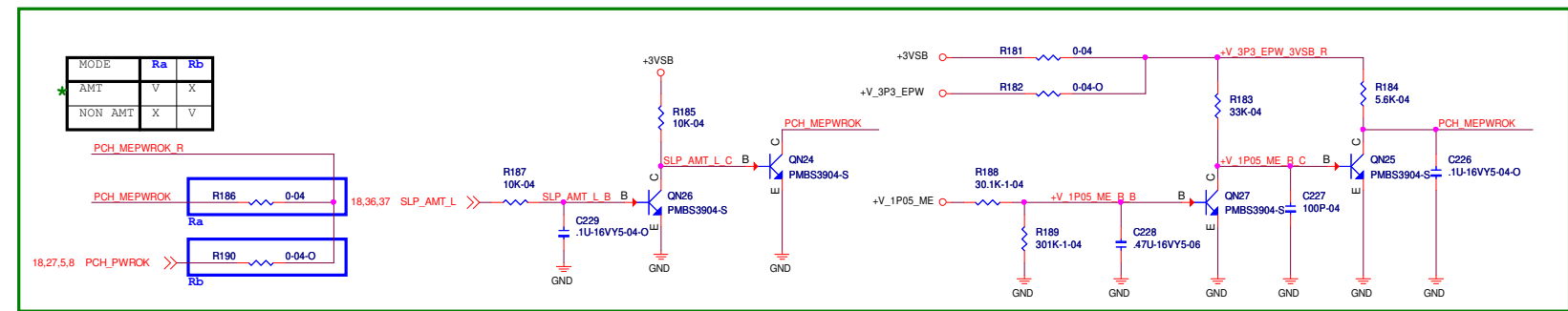
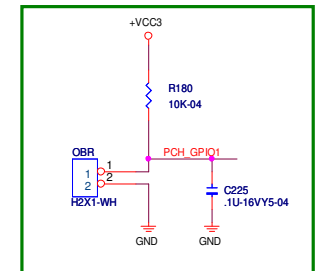
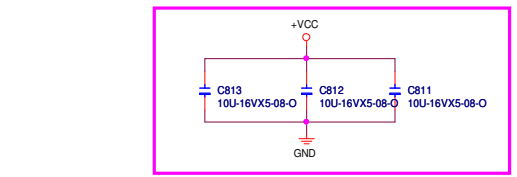
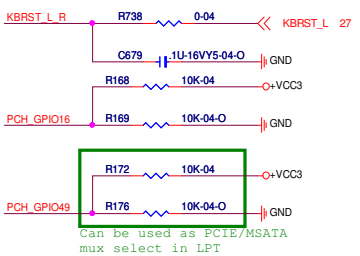
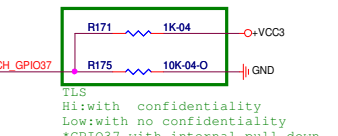
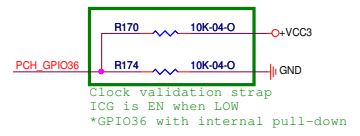
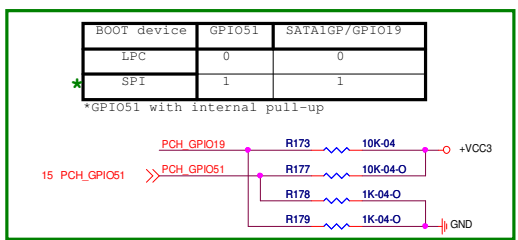
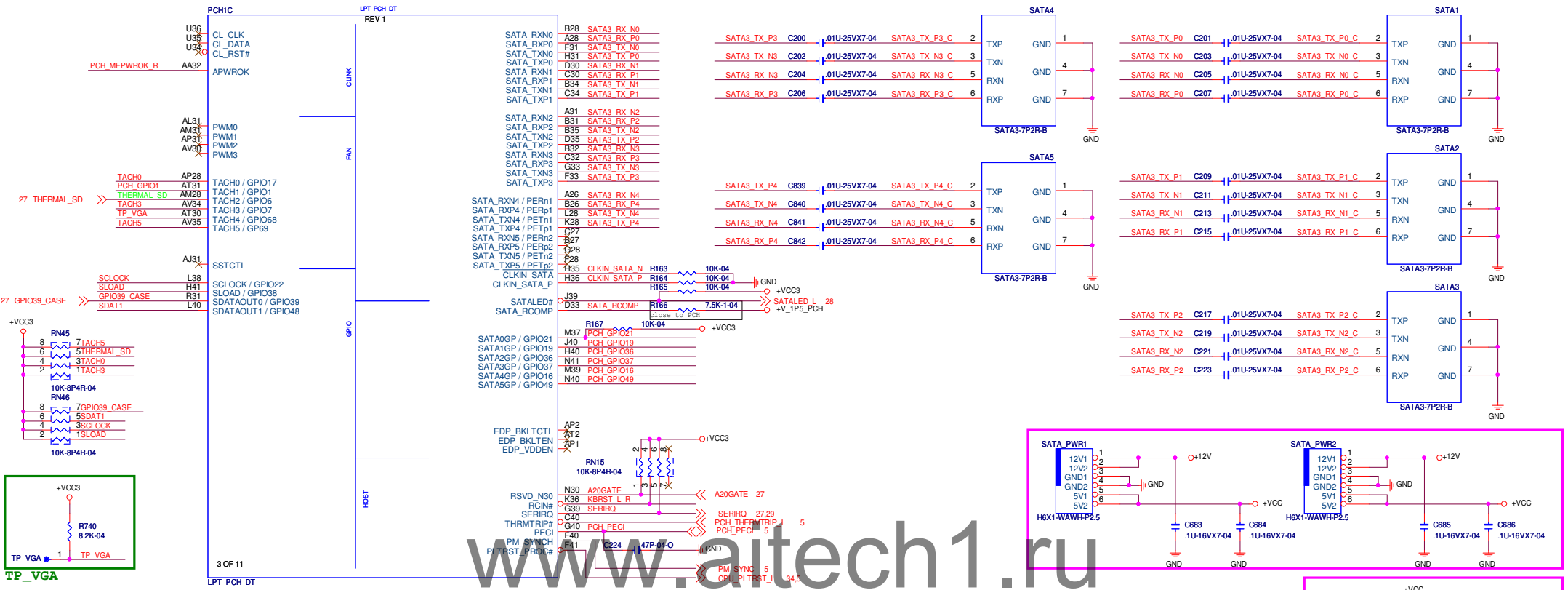
stitching caps for PEX16\_100M



stitching caps for single end clock

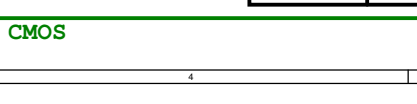
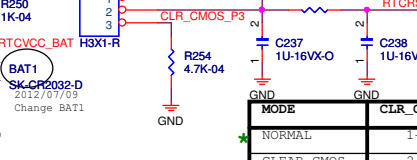
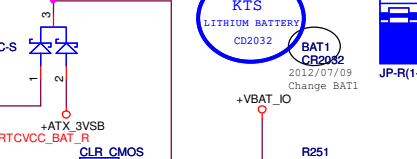
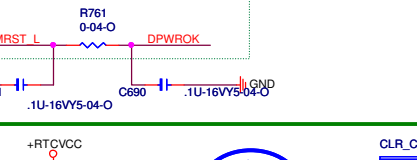
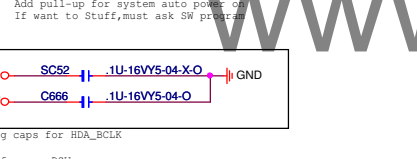
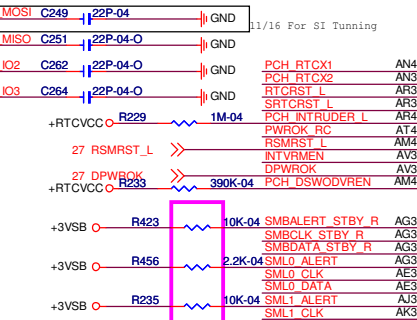
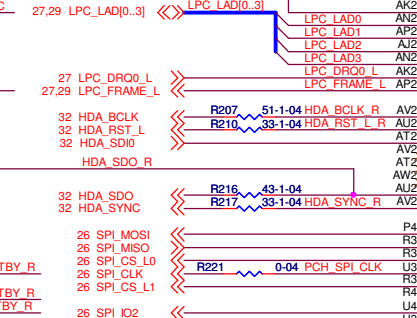
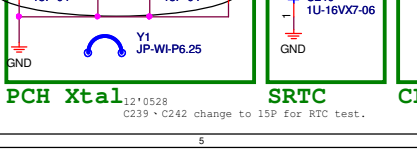
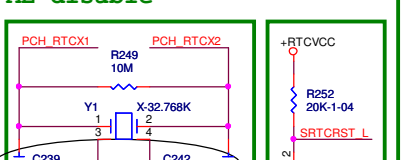
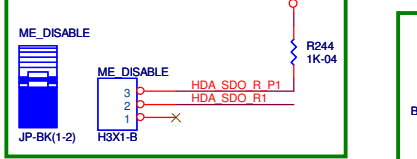
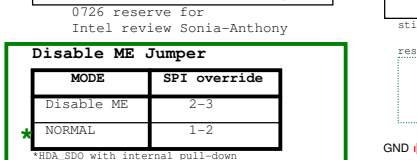
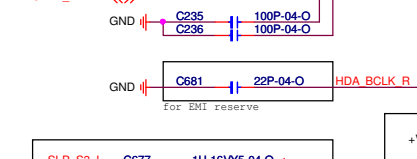
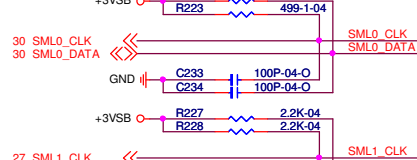
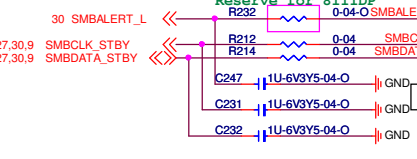
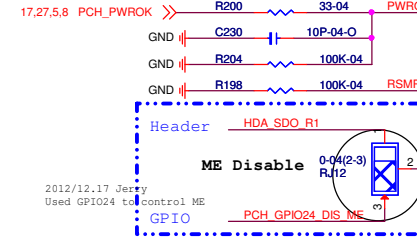
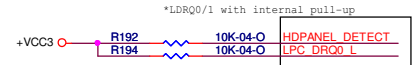


stitching caps for TCM 33M clock

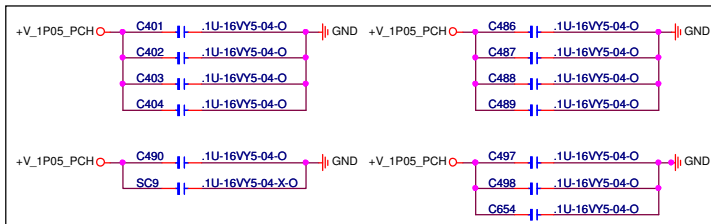
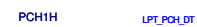


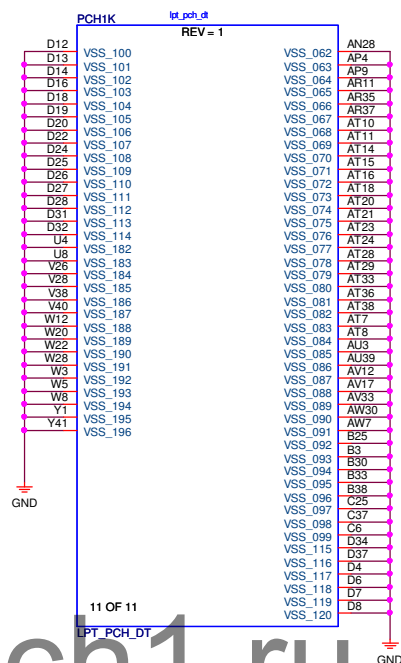
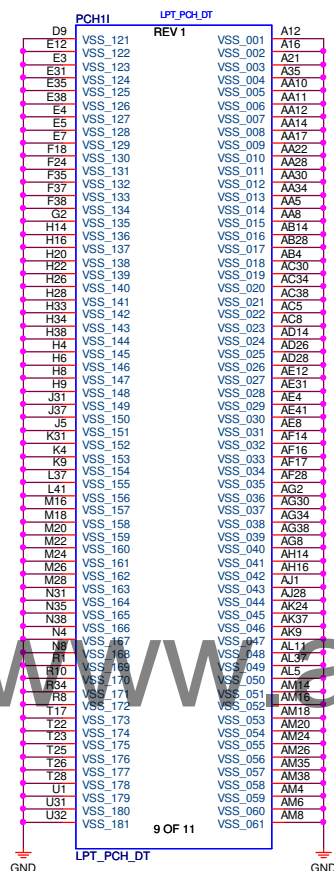
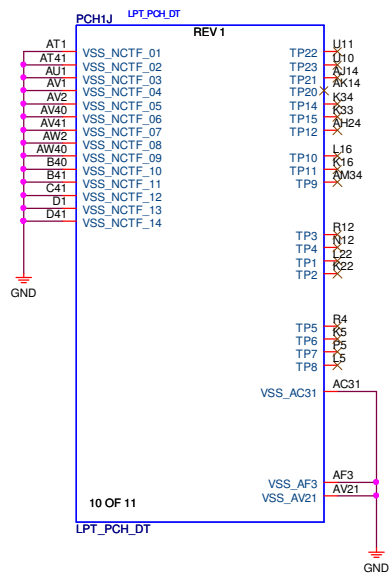
ME PWROK control circuit

PCH-SATA/SATA connector/OBR			
Size	Document Number	Rev	
Custom	Q87H3-AM	1.0	
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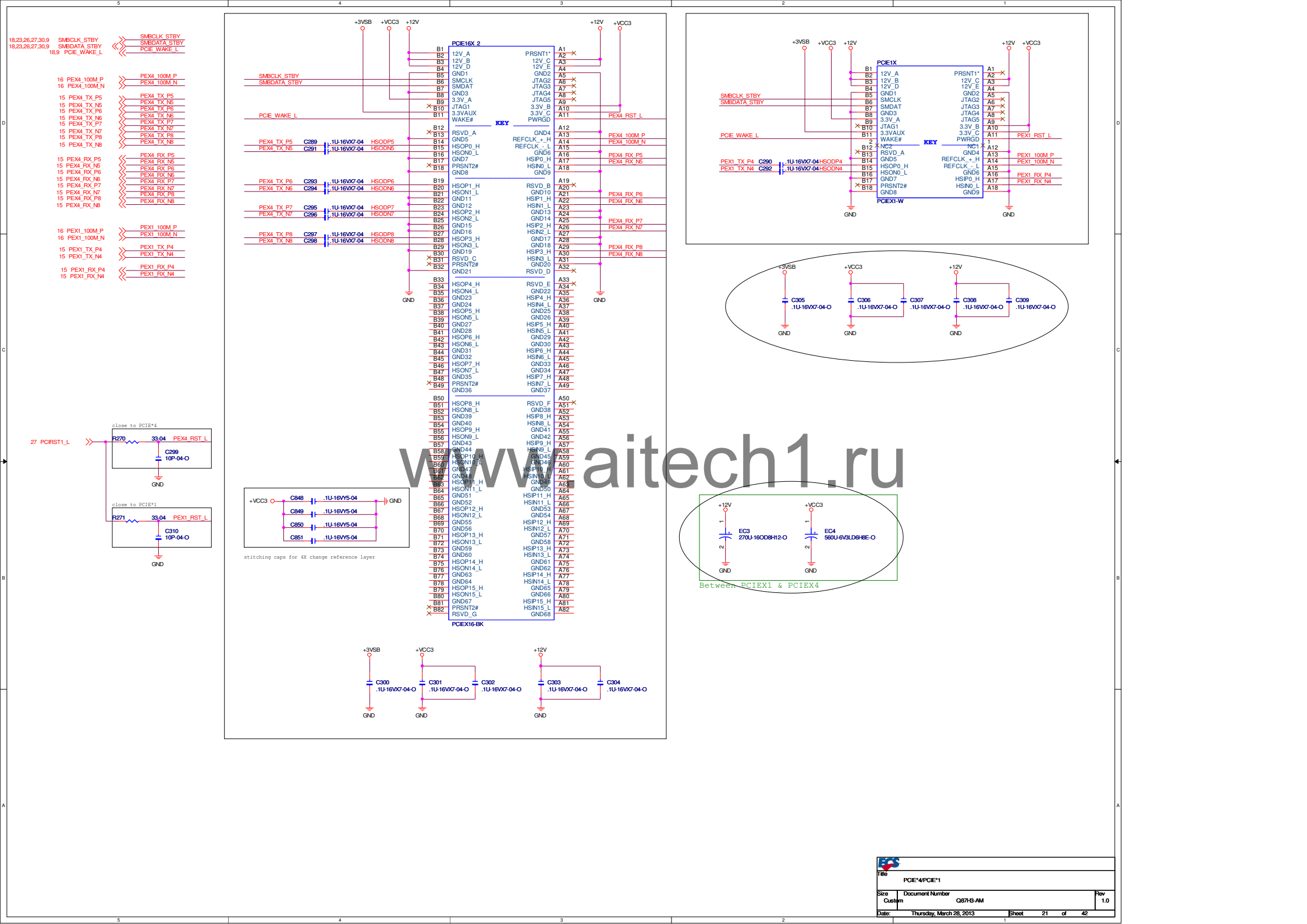






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22 AD[31..0] <<> AD[31..0]  
 22 C\_BE\_L[3..0] <<> C\_BE\_L[3..0]

22 GNT0\_L <<> GNT0\_L  
 22 REQ0\_L <<> REQ0\_L

22 INTA\_L <<> INTA\_L  
 22 INTB\_L <<> INTB\_L  
 22 INTC\_L <<> INTC\_L  
 22 INTD\_L <<> INTD\_L

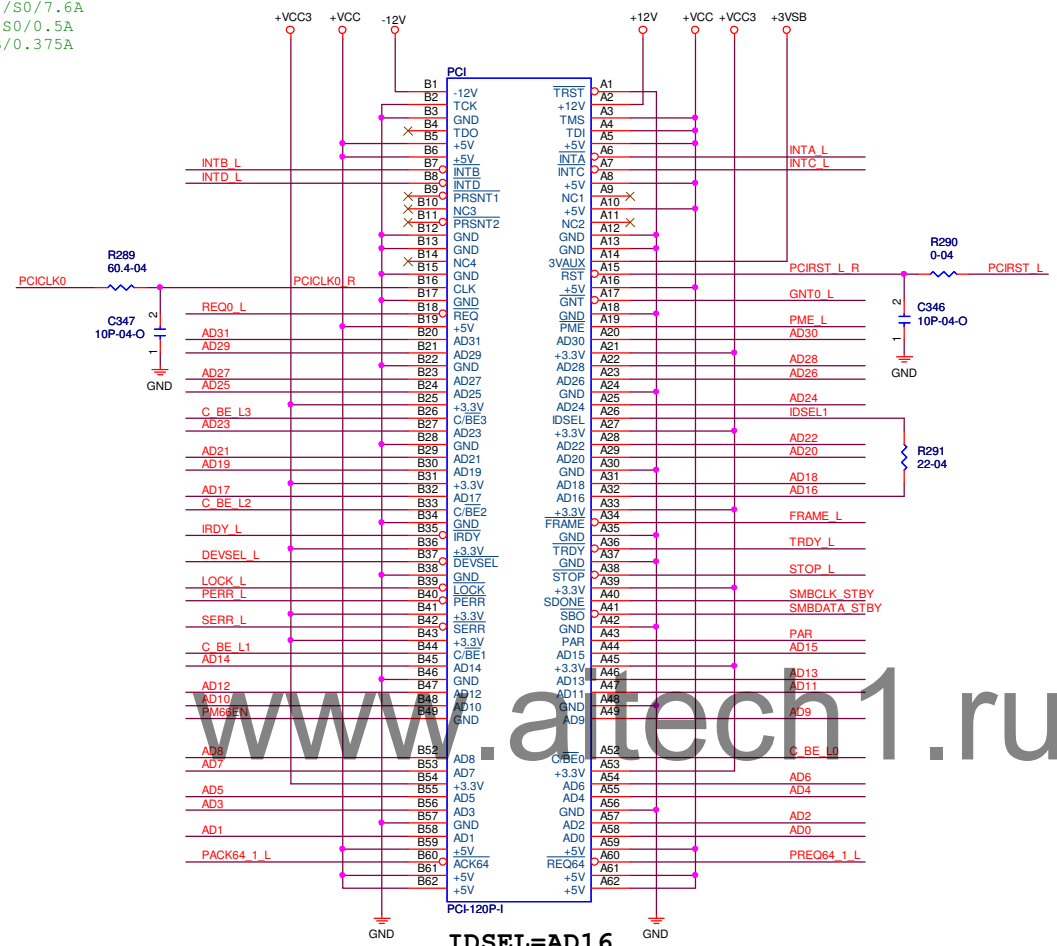
22 PAR <<> PAR  
 22 DEVSEL\_L <<> DEVSEL\_L  
 22 IRDY\_L <<> IRDY\_L  
 15 PME\_L <<> PME\_L  
 22 SERR\_L <<> SERR\_L  
 22 STOP\_L <<> STOP\_L  
 22 LOCK\_L <<> LOCK\_L  
 22 TRDY\_L <<> TRDY\_L  
 22 PERR\_L <<> PERR\_L  
 22 FRAME\_L <<> FRAME\_L

22 PCIRST\_L <<> PCIRST\_L  
 22 PCICLK0 <<> PCICLK0  
 22 PM66EN <<> PM66EN

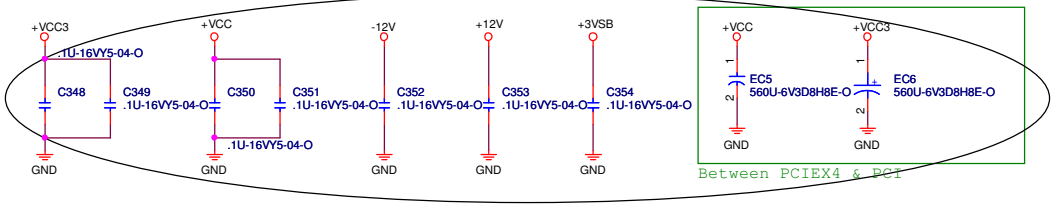
18,21,26,27,30,9 SMBCLK\_STBY <<> SMBCLK\_STBY  
 18,21,26,27,30,9 SMBDATA\_STBY <<> SMBDATA\_STBY

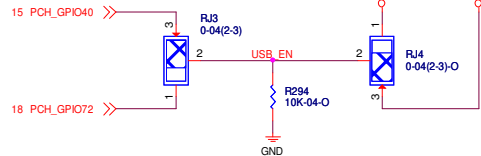
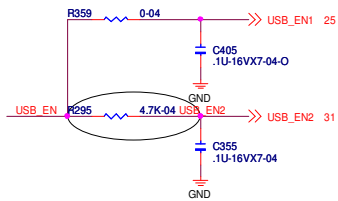
\*\*PCI Slot\*\*  
 +VCC/S0/5A  
 +VCC3/S0/7.6A  
 +V12/S0/0.5A  
 +3VSB/0.375A

+VCC3 R292 8.2K-04 PACK64\_1\_L  
 R293 8.2K-04 PREQ64\_1\_L

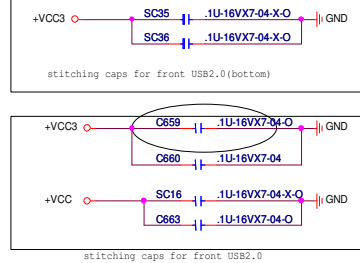


IDSEL=AD16  
 INT[A,B,C,D]





uP7536 Enable use	RJ?	RJ?	S4/S5 USB_5V_DUAL	Customer
VDIMM	0ohm (1-2)	NA	0 Volt	Acer S4 w/o S5 w/ USB_5VDUAL
5VSB	0ohm (2-3)	NA	5 Volt	
★ GPIO	NA	0 ohm	S4 : 0 Volt S5 : 5 Volt	



**Footprint: CMM21\_R0402**

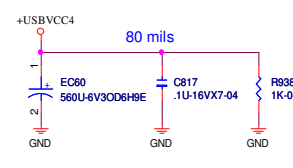
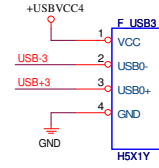
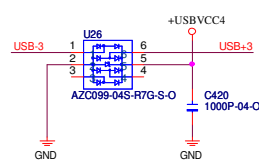
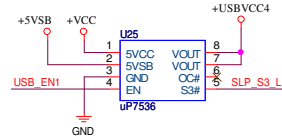
15 USB\_P3 <<> USB\_P3 4 3 USB+3

15 USB\_N3 <<> USB\_N3 1 2 USB-3

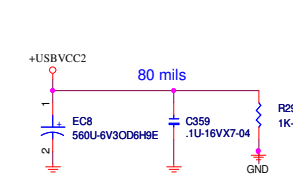
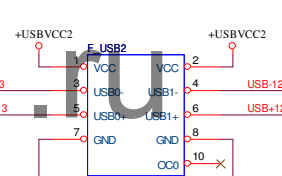
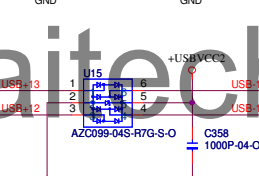
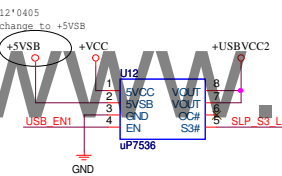
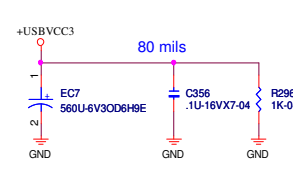
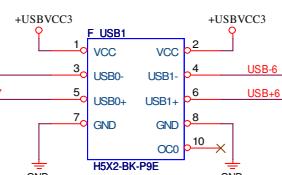
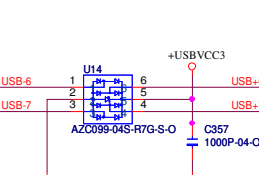
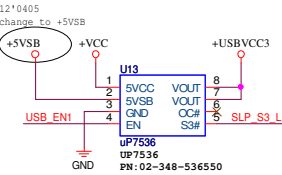
CMK37 CMK-90-08

**default上電阻, 位置為 CMK37 (1-2), CMK37 (3-4)**

V.B 上 Choke

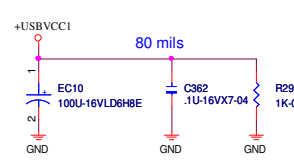
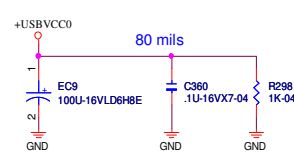
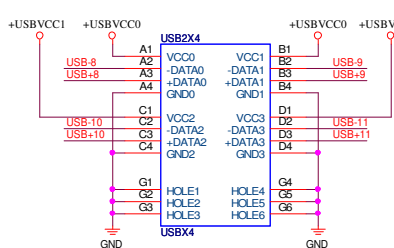
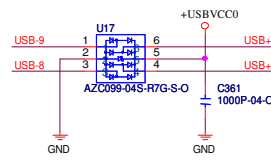
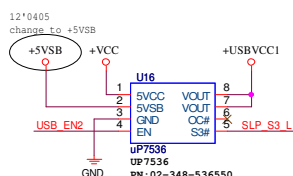
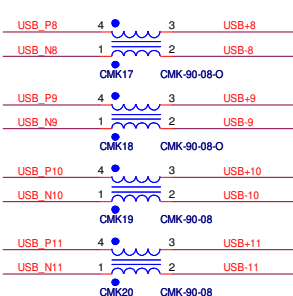
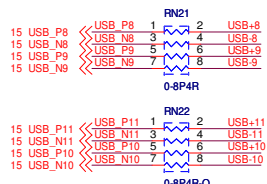


18,19,25,27,31,36,37,5 SLP\_S3\_L <<> SLP\_S3\_L

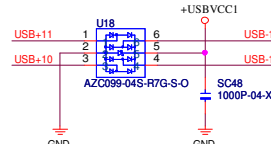


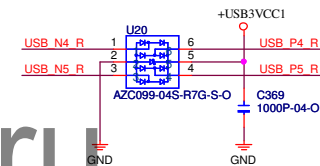
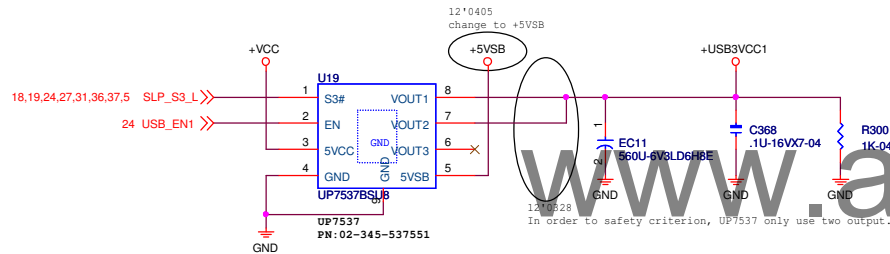
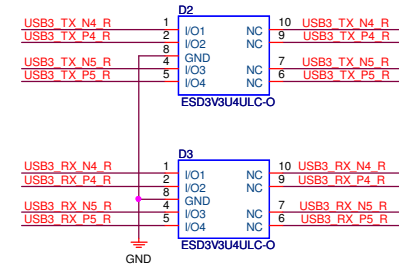
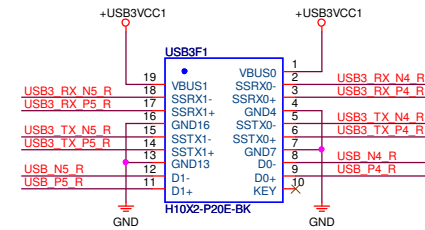
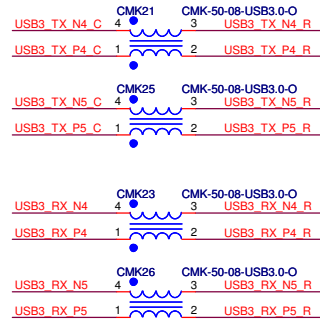
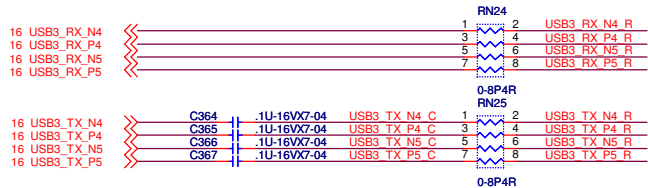
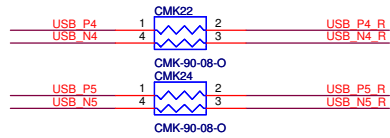
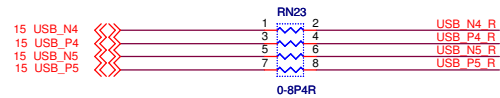
## USB2.0 header

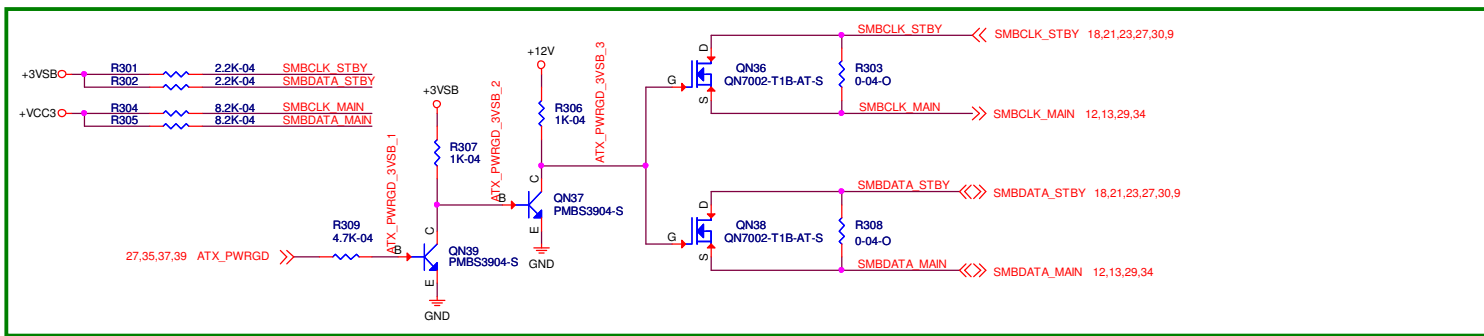
## USB2.0 connector



- OC[3:0]# should be connected with USB 2.0 ports 0 - 7 and any 4 of USB 3.0 ports 1 - 6.
- OC[7:4]# should be connected with USB 2.0 ports 8 - 13 and any 4 of USB 3.0 ports 1 - 6.

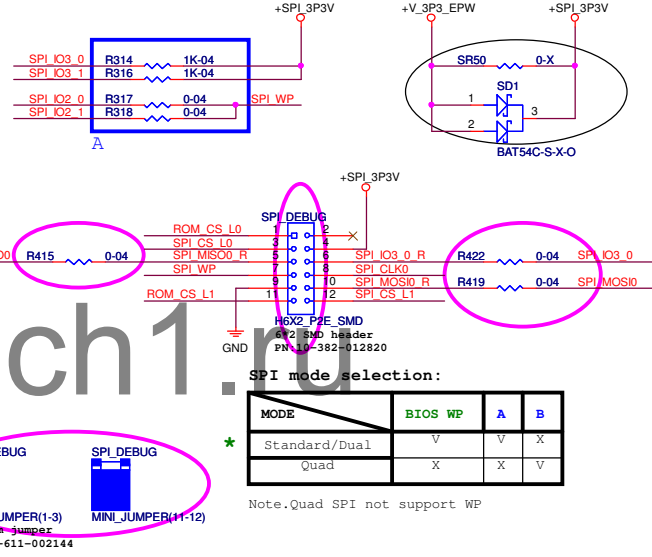
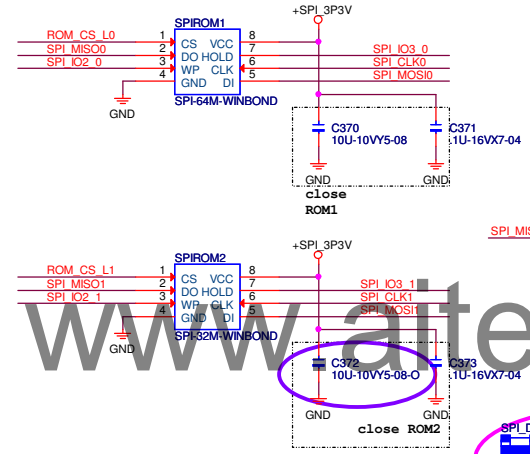
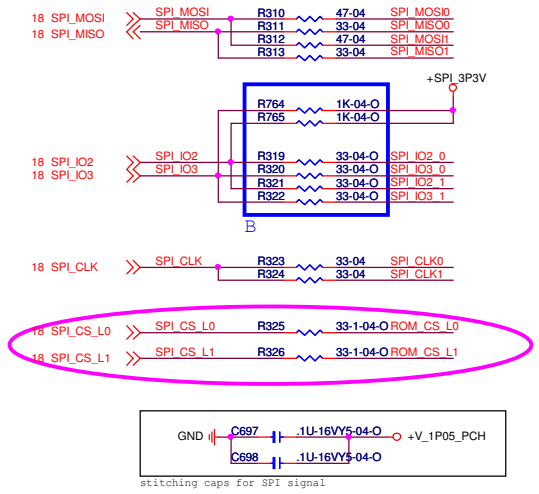






SMBus Logic Circuit

2013'03'20  
unstuff S01 change to SR50 for SPI Dubug board



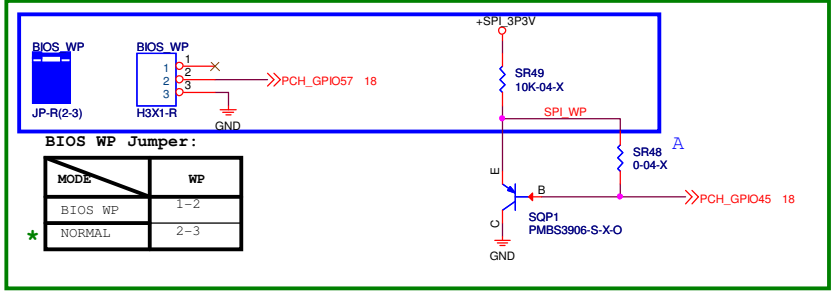
SPI mode selection:

MODE	BIOS WP	A	B
Standard/Dual	V	V	X
Quad	X	X	V

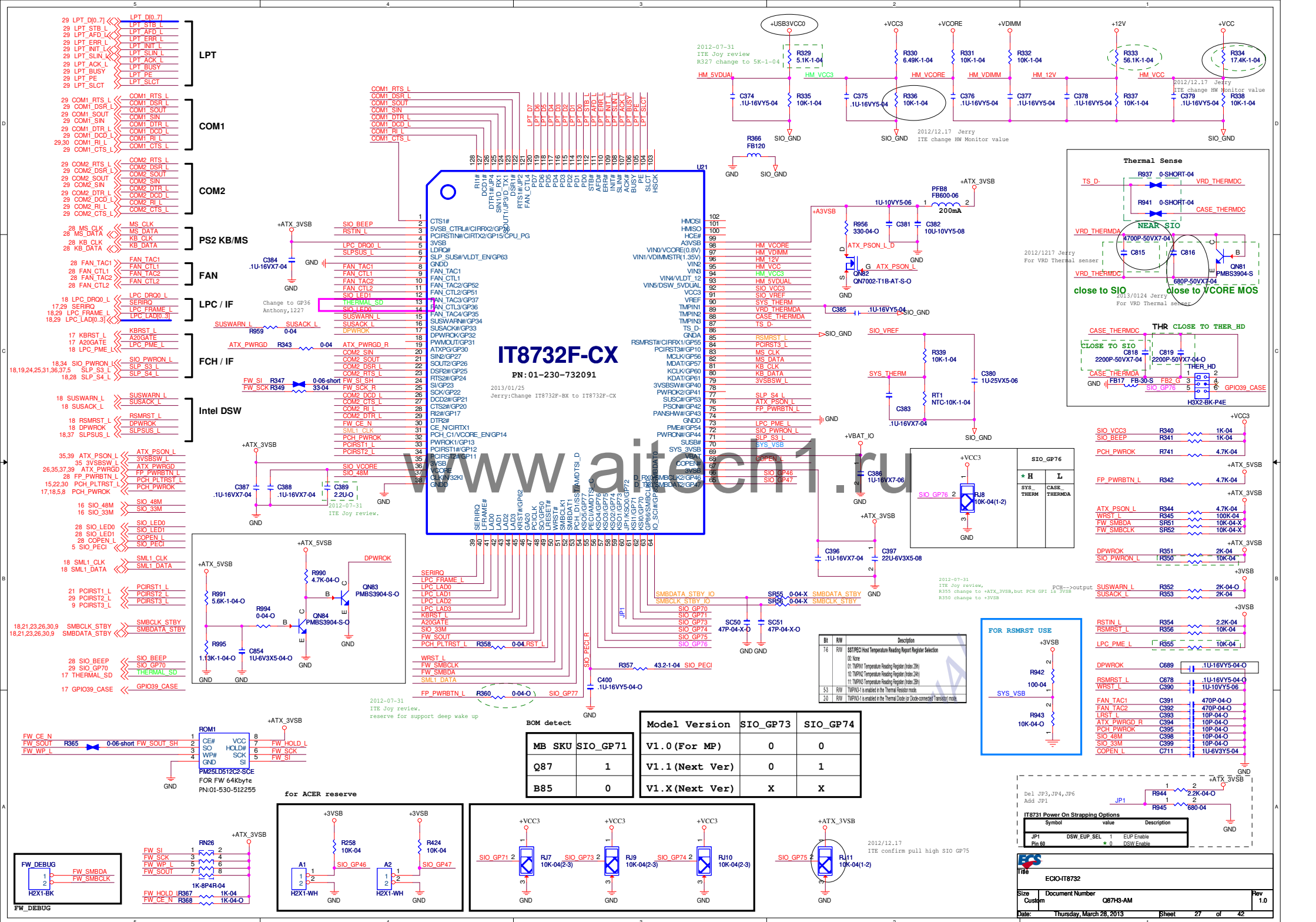
Note. Quad SPI not support WP

07/18 reserve for debug only-Anthony

SPI ROM



BIOS WP



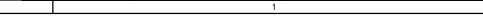






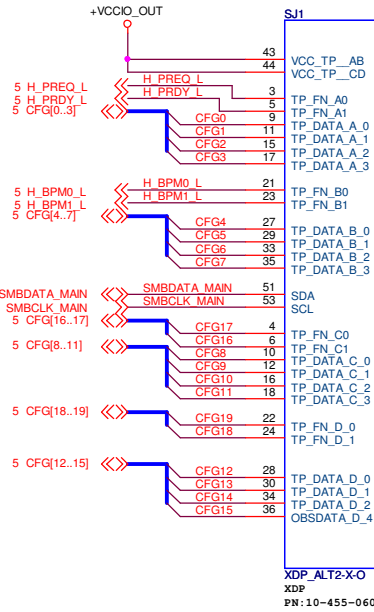
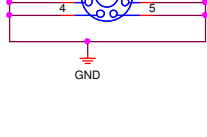
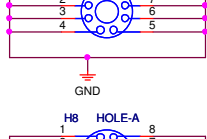
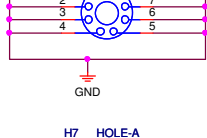
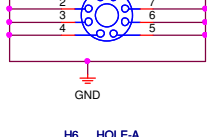
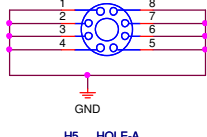
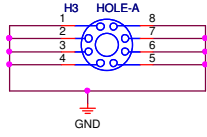
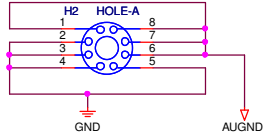
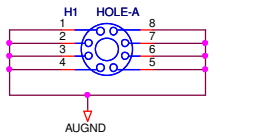




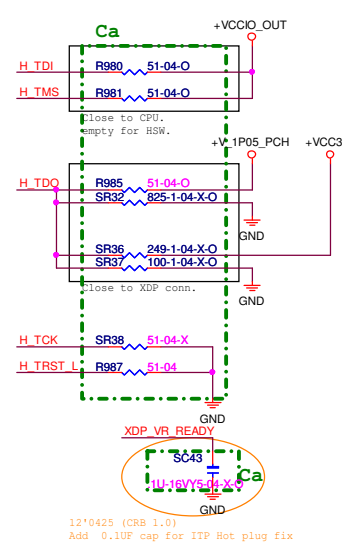
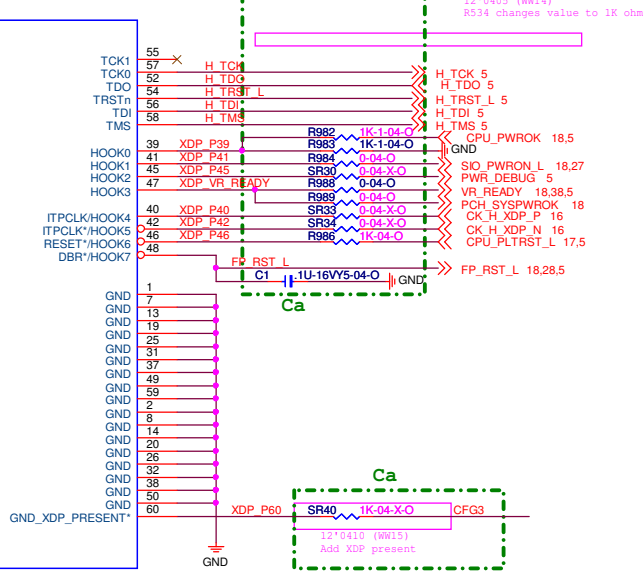








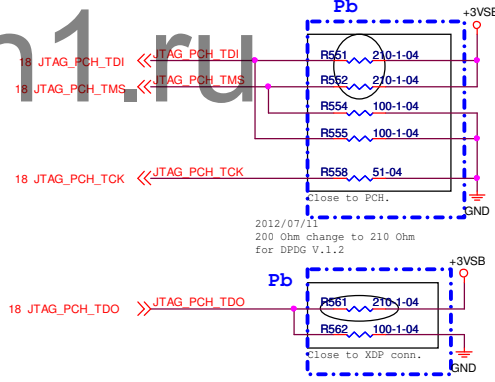
XDP  
PN:10-455-060722



	Ca
CPU XDP function	V
NO CPU XDP function	X

-O:報價

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	Pb
PCH XDP function	V
NO PCH XDP function	X

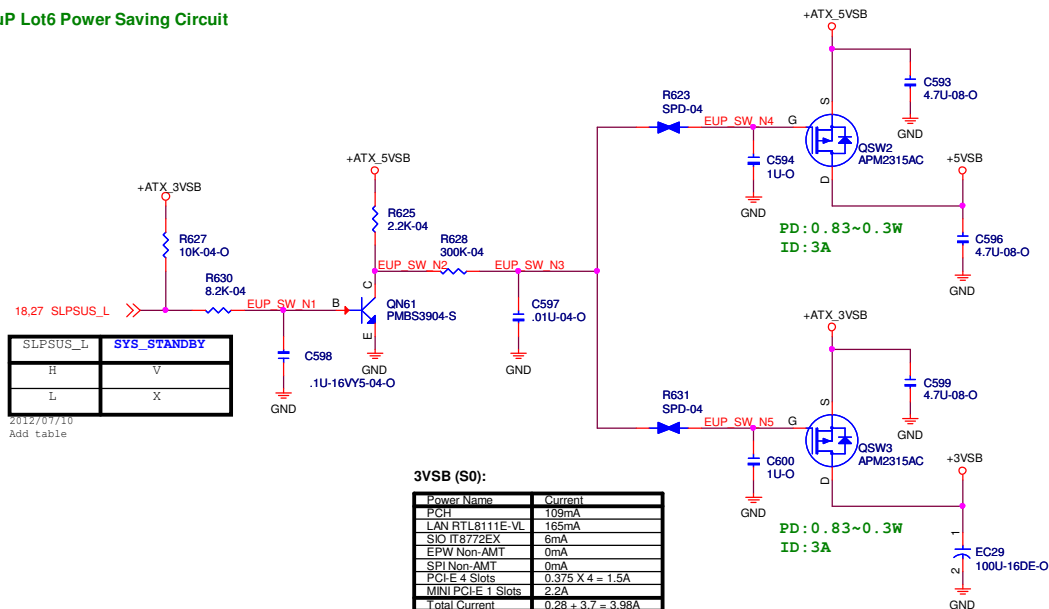




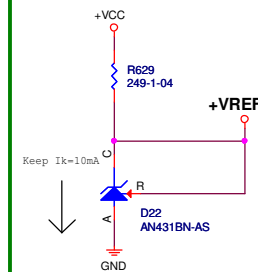
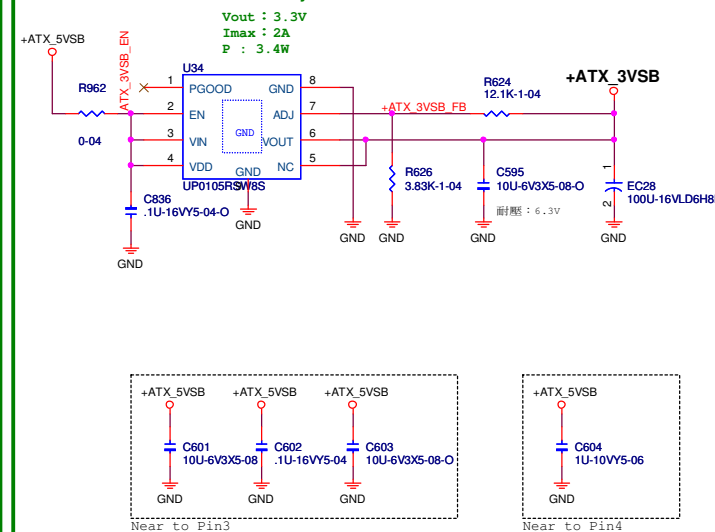




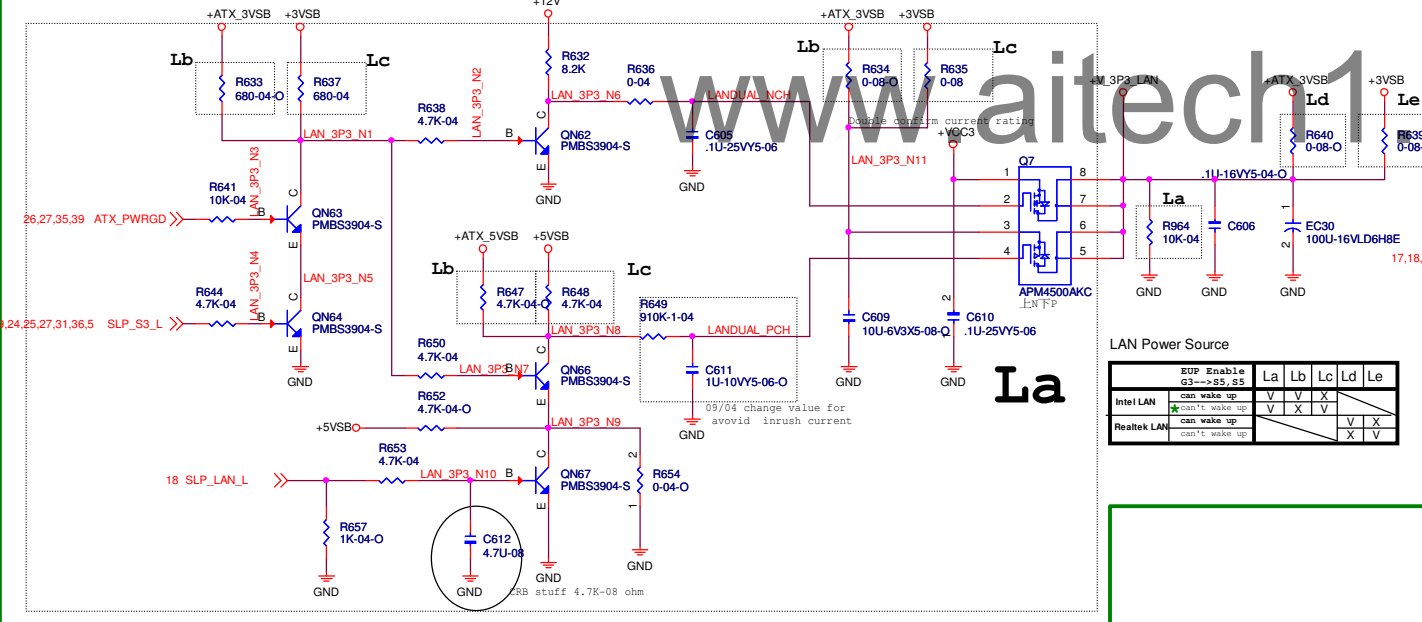
## EuP Lot6 Power Saving Circuit



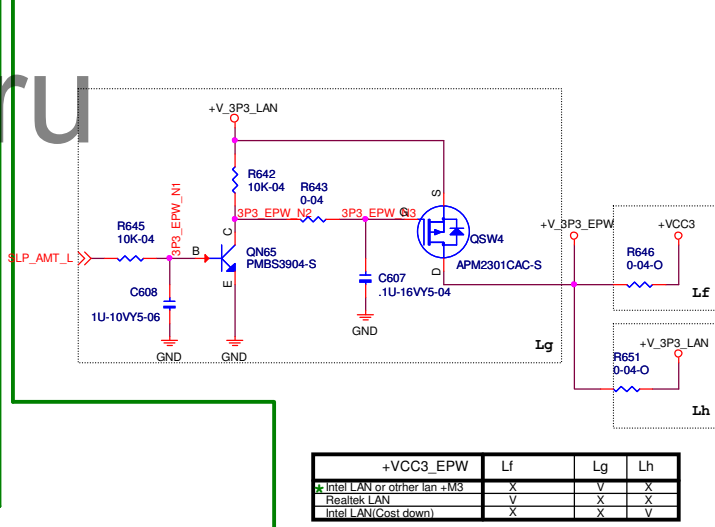
## +3V Standby



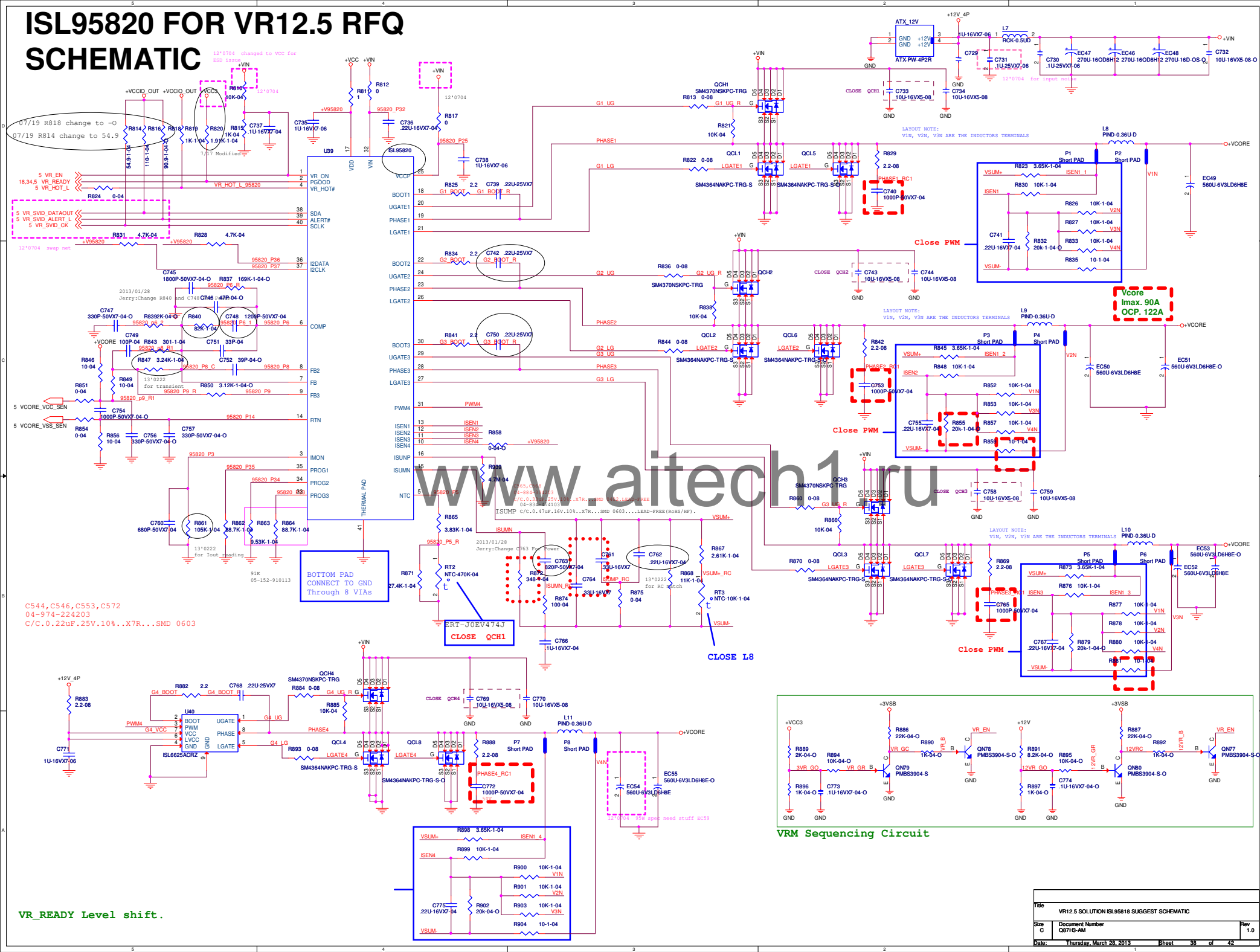
## LAN Power Circuit



## SPI ROM & PCH Power Circuit



# ISL95820 FOR VR12.5 RFQ



VR\_READY Level shift.

### VRM Sequencing Circuit

Title				
VR12.5 SOLUTION ISL95818 SUGGEST SCHEMATIC				
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C	Q87H3-AM			1.0
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